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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,517	KUO, CHIA-CHU	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9-12,14-16 and 18-20* is/are rejected.

7)☒ Claim(s) *3,8,13 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant' Amendment and RCE filed September 14, 2006. Claims 1-20 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1,2,4-5,7,9-10,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura (6,435,869) taken with Kobayashi et al (6,200,432).

Re claims 1,7,12, Kitamura teaches a method for annealing a semiconductor substrate, the method comprising: providing a single wafer processing furnace (single wafer "W" as shown in Fig 1); turning on at least one heat source 130 coupled to the single wafer processing furnace (Figs 1,2,9; col 5, line 45 through col 7); heating a semiconductor substrate W in the chamber; turning off the at least one heat source (Figs 1,2,9,21-24; col 17, lines 30-54); cooling the semiconductor substrate in the chamber; wherein the heating a semiconductor substrate includes raising a temperature of the semiconductor substrate from a first temperature value to a second temperature value; the cooling the semiconductor substrate (col 14, lines 46-68)includes lowering the temperature of the semiconductor substrate from the second temperature value to a third temperature value; the heating a semiconductor substrate includes absorbing an energy from the at least one heat source by the semiconductor substrate; the cooling the semiconductor substrate includes flowing a first gas of helium gas in a vicinity of the substrate W, wherein the gas is also flowed into at least one wall of the chamber (Figs 20-24; col 17, lines 30-48; col 13, lines 35-60; col 16, lines 25-35), flowing a second gas in a vicinity of the at least one heat source 130 (Figs 9,2-3; col 8, lines 49-65; col 6, lines 30-35), and flowing a third gas of helium gas in a vicinity of the semiconductor substrate W (Fig 24; col 17, lines 30-48); a first temperature of the first gas is lower than the second temperature value; a second temperature of the second gas is lower than the second temperature value; a third temperature of the third gas is lower than the second temperature value (col 16, line 14 through col 17, line 48); and wherein the first temperature of the first gas, the second temperature of the second gas, and the third temperature of the third gas are temperature of the cooling air (i.e. room temperature). Re claim 2, wherein the first temperature, the second temperature, and the third temperature of the coolant gases, such

as helium gas, each is lower than the third temperature value (col 16, line 14 through col 17, line 48; col 12, line 66 through col 13). Re claims 4,9,14, wherein the first gas, the second gas, and the third gas each comprise at least one selected from a group consisting of nitrogen and helium (col 13, lines 52-60 and Figure 20). Re claims 5,10, wherein the method further comprises maintaining the temperature of the semiconductor substrate at the second temperature value for a time period (col 17, lines 30-47). Re further claim 12, wherein the heat source comprises at least one lamp 130 (Figs 8-9; col 8, lines 55-65).

Kitamura thus lacks using the cooling gas at below room temperature.

However, Kobayashi teaches (at col 9, lines 55-62) using a cooling gas at room temperature or at a temperature lower than room temperature for enhancing the cooling effect.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the cooling method of Kitamura by using a cooling gas at room temperature or at a temperature lower than room temperature as taught by Kobayashi. This is because of the desirability to further enhance the cooling effect, thereby reduce the cooling time.

2. Claims 6,11,15-16,18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura (6,435,869) and Kobayashi et al (6,200,432), as applied to claims 1,2,4-5,7,9-10,12,14 above, and further of Suzuki (2004/0009644).

The references including Kitamura and Kobayashi teaches a method for annealing a semiconductor substrate by rapid heating a semiconductor substrate with the lamps 130, and rapid cooling by using coolant gases as applied to claims 1,2,4-5,7,9-10,12,14 above. Re claim 16, wherein the first temperature, the second temperature, and the third temperature of the coolant gases, such as helium gas, each is lower than the third temperature value (col 16, line 14 through col 17, line 48; col 12, line 66 through col 13). Re claim 18, wherein the first gas, the second gas, and the third gas each comprise at least one selected from a group consisting of nitrogen and helium (col 13, lines 52-60 and Figure 20). Re claim 19, wherein the method further comprises maintaining the temperature of the semiconductor substrate at the second temperature value for a time period (col 17, lines 30-47).

Re claims 6,11,15, Kitamura also teaches (at col 1, lines 13-27) about annealing a semiconductor substrate, but lacks mentioning the semiconductor substrate comprises a source

region and a drain region, the source region including a source LDD region, the drain region including a drain LDD region. Re claim 20, wherein the first temperature value equals to the third temperature value.

However, re claims 6,11,15, Suzuki teaches (at Figs 4D-4H; paragraphs 7-15) about annealing and cooling a semiconductor substrate, wherein the semiconductor substrate comprises a source region and a drain region, the source region including an extended source LDD region 8a (Figs 4D-4E), the drain region including an extended drain LDD region 8b (Figs 4D-4E; paragraph 9). Re claim 20, as shown in Figs 3 and 5, Suzuki also teaches to heat the semiconductor substrate from an initial first temperature value, and to cool down the semiconductor substrate back to about the same first initial temperature value as the third temperature value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to manufacture and anneal the semiconductor substrate of Kitamura to comprise a MOS semiconductor device having a source region and a drain region, the source region including a source LDD region, the drain region including a drain LDD region, as taught by Suzuki. This is because of the desirability to form a field effect semiconductor MOS transistor, through miniaturization, that can be operated at high speed with low power consumption, wherein the extended LDD source and drain regions also suppress short channel effect. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to cool the semiconductor substrate of Kitamura back to the initial first temperature value as taught by Suzuki. This is because of the desirability to cool the semiconductor substrate to an initial temperature so that the substrate can be removed from the chamber into the fabrication areas.

3. Claims 7,9,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waugh (4,802,441) taken with Kobayashi et al (6,200,432).

Waugh teaches a method for annealing a semiconductor substrate, the method comprising: providing a wafer processing furnace, which furnace can be easily inherently accommodated at least a single wafer and up to a plurality of wafers for batch processing (e.g. up to 250 wafers at col 6, lines 1-68), wherein the furnace inherently and obviously enables

processing of a single wafer when necessary; heating at least a semiconductor substrate 44 in a chamber (e.g. 44 in Fig 2, col 4, lines 4-22; Fig 5, col 6, line 57 through col 7); cooling the semiconductor substrate in the chamber (Fig 2, Fig 5); wherein the heating a semiconductor substrate includes raising a temperature of the semiconductor substrate from a first temperature value (i.e. temperature of the wafer before loading into the chamber) to a second temperature value (col 1, lines 25-45; col 6, line 57 through col 7; 1000 or 800 degrees centigrade); the cooling the semiconductor substrate includes lowering the temperature of the semiconductor substrate from the second temperature value to a third temperature value (col 1, lines 25-45; col 6, line 57 through col 7; 600 or 200 or 150 degree centigrade); the heating a semiconductor substrate includes absorbing an energy from at least one heat source 18 by the semiconductor substrate 44 (col 3, lines 18-34; Figs 1,2); the cooling the semiconductor substrate includes flowing a first gas 61,63 of N_2 in a vicinity of at least one wall of the chamber, flowing a second gas 61 in a vicinity of the at least one heat source 18 and flowing a third gas 63 in a vicinity of the semiconductor substrate 44 (Figs 1-2); a first temperature of the first gas is lower than the third temperature value; a second temperature of the second gas 61 is lower than the third temperature value; a third temperature of the third gas 63 is lower than the third temperature value (Fig 1-2; col 4, lines 35-45; lines 4-68; col 7, lines 29-60; col 1, lines 25-45); and wherein the first temperature of the first gas, the second temperature of the second gas, and the third temperature of the third gas are temperature of the cooling air (i.e. room temperature). Re claim 9, wherein the gases comprise nitrogen (N_2 at col 7, lines 29-60). Re claim 10, wherein the semiconductor substrate is maintained at the second temperature value e.g. at round 1000 degrees centigrade during gate oxide formation process (col 1, lines 25-45).

Waugh thus lacks using the cooling gas at below room temperature.

However, Kobayashi teaches (at col 9, lines 55-62) using a cooling gas at room temperature or at a temperature lower than room temperature for enhancing the cooling effect of a single wafer in a single wafer processing furnace (e.g. single wafer 10 on cooling stage 33 and 13 in Fig 2)

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the cooling method of Waugh by using a cooling gas at room

temperature or at a temperature lower than room temperature as taught by Kobayashi. This is because of the desirability to further enhance the cooling effect, thereby reduce the cooling time.

Regarding a single wafer furnace, although the wafer furnace of Waugh is preferably used for batch processing a plurality wafers, a single wafer can be loaded in the furnace and processed when needed. Thus, it would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the furnace of Waugh for processing at least a single wafer, when needed, so as to reduce cost rather than buying an additional furnace for a single wafer.

Allowable Subject Matter

4. As already of record, claims 3,8,13,17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

5. Applicant's remarks with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

*** Regarding Waugh (4,802,441): Applicant remarked that the furnace is for "batch processing".

In response, although it is preferably to batch process a plurality of wafers in the furnace during production, the furnace still enables to process a few wafers including a single wafer when needed by vertically loaded a single wafer in the furnace. Thus, by process a single wafer, it is a single wafer processing furnace.

*** Regarding Kitamura (6,435,869): Applicant remarked about the furnace of Kitamura that having "...quartz window reinforced with ribs...".

In response, this is noted and found unconvincing. Kitamura clearly teaches the claimed invention directed to the method of annealing, wherein a single wafer furnace (single wafer "W" as shown in Figure 1) is provided. The claims directed to a method of annealing should be distinguished from the prior art in terms of method of annealing rather than the apparatus itself.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-17

Michael Trinh
Primary Examiner